# 1 Description

The USB Blaster Download Cable interfaces a USB port on a host computer to an Altera® FPGA mounted on a printed circuit board. The cable sends configuration data from the PC to a standard 10-pin header connected to the FPGA. You can use the USB Blaster cable to iteratively download configuration data to a system during prototyping or to program data into the system during production.

It surpports the ALTERA total series FPGA/CPLD devices, Active Serial Configuration Devices, Enhanced Configuration Devices, and supports AS, PS, JTAG three download modes.

# 2 Features

**Performance**

- Supports ALTERA total series FPGA/CPLD devices.
- Supports ALTERA total series Active Serial Configuration Devices.
- Supports ALTERA total series Enhanced Configuration Devices.
- Supports AS, PS, JTAG three download modes.
- High-speed, stable, and internal FT245R+CPLD designed.
- Supports 1.2-5V programming voltage.
- Supports SignalTap II embedded logic analyzer.
- Supports Nios II of embedded processor communication and debugging.

**Supported Software**

- Quartus II integrated development environment.
- NIOS II IDE integrated development environment.
- NIOS II EDS integrated development environment.

**Supported Devices**

- CPLD: MAX3000, MAX7000A/B/S, MAX9000 and MAX II etc.
- FPGA: Stratix, Stratix II, Cyclone, Cyclone II, CycloneIII, ACEX 1K, APEX 20K and FLEX 10K etc.
- Active Serial Configuration Devices including: EPCS1, EPCS4, EPCS16 etc.
- Enhanced Configuration Devices including: EPC1, EPC4 etc.

**Other Features**

- High download speed: FT245+CPLD+244, close to the original ALTERA USB Blaster.
- Download speed 1-3 times faster than other schemes, such as 68013 or C8051F.

**Connects to PC**

- Computer connection via USB 2.0 interface.

**Connects to target board**

- Target board connection via JTAG, AS, PS interfaces. The figure 1, 2,and 3 below shows the header pinouts of different interfaces. Table 1 shows more details for corresponding programming modes.

**Figure 1.** JTAG header pinout

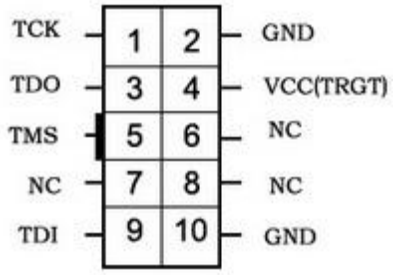


**Figure 2.** AS header pinout

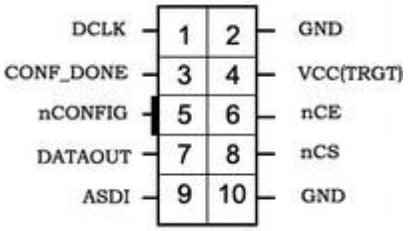


**Figure 3.** PS header pinout

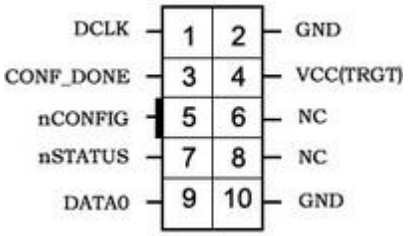


**Table 1.** Signal Names & Programming Modes

| Pin | AS Mode | | PS Mode | | JTAG Mode | |
|---|---|---|---|---|---|---|
| | Signal Name | Description | Signal Name | Description | Signal Name | Description |
| 1 | DCLK | Clock signal | DCLK | Clock signal | TCK | Clock signal |
| 2 | GND | Signal ground | GND | Signal ground | GND | Signal ground |
| 3 | CONF_DONE | Configuration done | CONF_DONE | Configuration done | TDO | Data from device |
| 4 | VCC (TRGT) | Target power supply | VCC (TRGT) | Target power supply | VCC (TRGT) | Target power supply |
| 5 | nCONFIG | Configuration control | nCONFIG | Configuration control | TMS | JTAG state machine control |
| 6 | nCE | Cyclone chip enable | — | No connect | — | No connect |
| 7 | DATAOUT | Active serial data out | nSTATUS | Configuration status | — | No connect |
| 8 | nCS | Serial configuration device chip select | — | No connect | — | No connect |
| 9 | ASDI | Active serial data in | DATA0 | Data to device | TDI | Data to device |
| 10 | GND | Signal ground | GND | Signal ground | GND | Signal ground |

# 3 LED Status

- Red LED: Power indicator
- Green LED: Signal indicator, the LED is on while downloading/programming

For more info, please refer to the ALTERA official datasheet "ug_usb_blstr", which is also provided in our CD(DVD_ALTERA_EN\data\Datasheets\USB Blaster).